BUK9Y4R8-60RA

N-channel 60 V, 4.8 mOhm logic level MOSFET in LFPAK56 using Repetitive Avalanche technology

11 October 2024 **Product data sheet**

1. General description

Logic level N-channel MOSFET in an LFPAK56 (Power SO8) package using Application Specific (ASFET) repetitive avalanche silicon technology. This product has been designed and qualified to AEC-Q101 for use in repetitive avalanche applications.

2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Repetitive Avalanche rated to 30 °C T_j rise:
  - Tested to 1 Bn avalanche events
- LFPAK copper clip package technology:
  - High robustness and reliability
  - Gull wing leads for high manufacturability and AOI

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Repetitive avalanche topologies
- Engine control
- Transmission control
- Actuator and auxiliary loads

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	60	V
I_D	drain current	V_{GS} = 5 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	100	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	238	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A; T_j = 25 °C; Fig. 14		-	3.3	4.8	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 48 V; V_{GS} = 5 V; T_j = 25 °C; Fig. 16; Fig. 17		-	18.1	-	nC
Source-drain diode							
Q_r	recovered charge	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V; T_j = 25 °C		-	28	-	nC

[1] Continuous current is limited by package.

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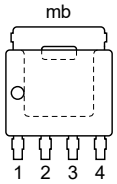
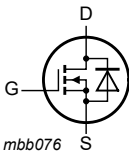
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 **LFPAK56; Power-SO8 (SOT669)**	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9Y4R8-60RA	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Y4R8-60RA	94RA860

8. Limiting values

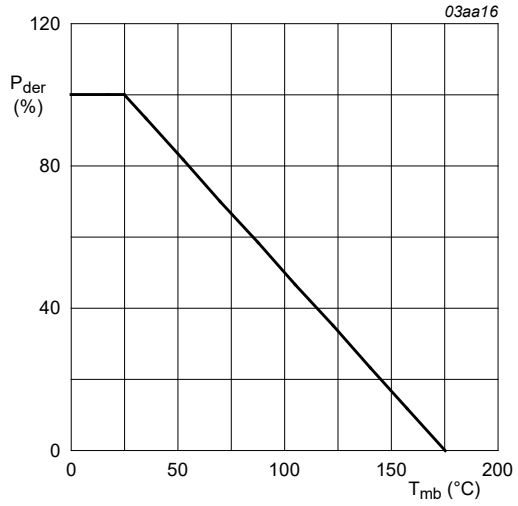
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	60	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ		-	60	V
V_{GS}	gate-source voltage			-16	16	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	238	W
I_D	drain current	V_{GS} = 5 V; T_{mb} = 25 °C; Fig. 2	[1]	-	100	A
		V_{GS} = 5 V; T_{mb} = 100 °C; Fig. 2	[1]	-	100	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	593	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[1]	-	100	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	593	A

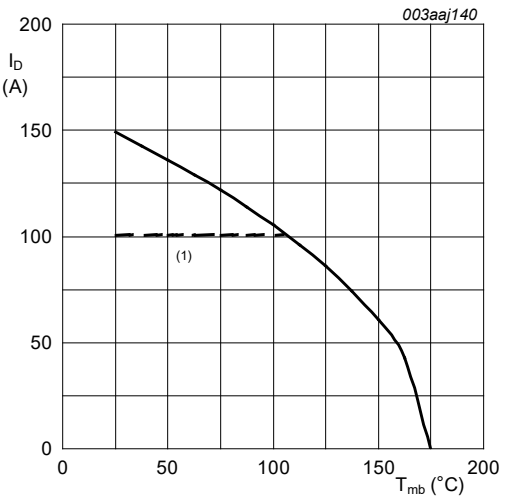
Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	I_D = 4.9 A; $V_{sup} \leq$ 60 V; R_{GS} = 10 Ω; V_{GS} =10 V; $T_{j(rise)} \leq$ 30 °C; unclamped; Fig. 4; Fig. 5; Fig. 6	[2] [3] [4]	-	189	mJ
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 100 A; $V_{sup} \leq$ 60 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 7	[5] [6]	-	199	mJ

[1] Continuous current is limited by package.
[2] Repetitive avalanche rating is limited by maximum junction temperature of 175 °C and junction rise of 30 °C
[3] Refer to Fig. 5 for the limiting number of avalanche events
[4] Refer to Fig. 6 Rdson at Vgs=5V will increase as a function of repetitive avalanche cycles
[5] Refer to application note AN10273 for further information
[6] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



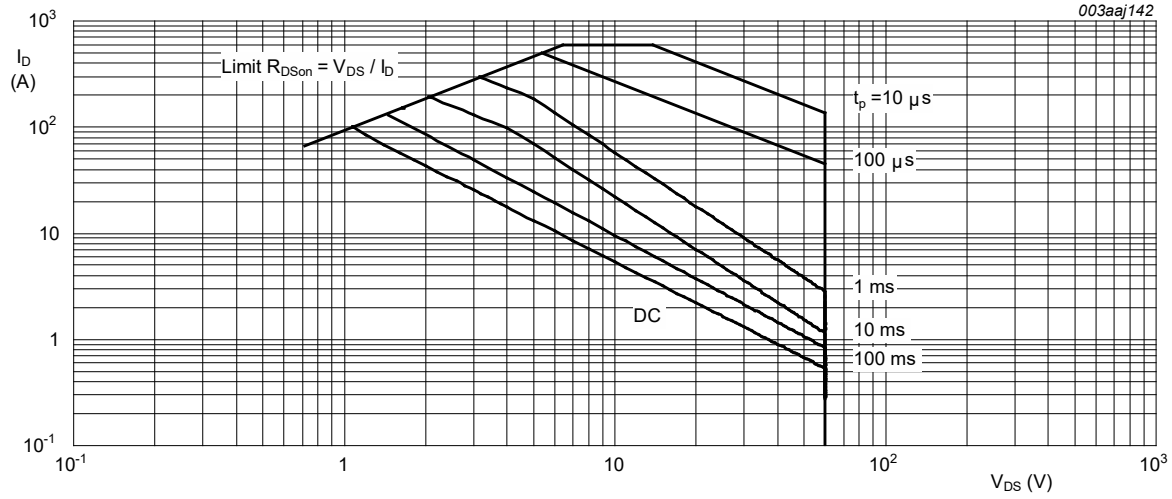
$$P_{der} = \frac{P_{tot}}{P_{tot\,(25\,°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



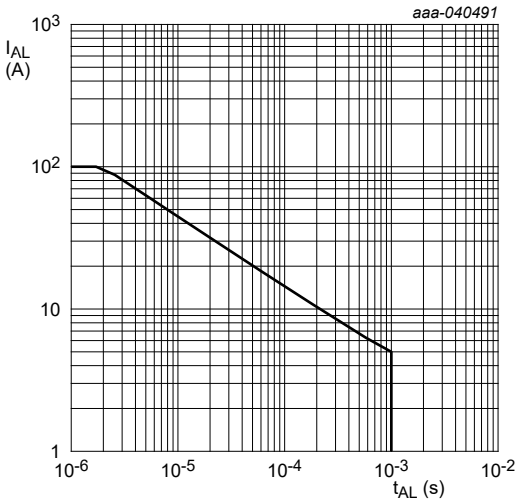
(1) Capped at 100A due to package
$V_{GS} \geq 5V$

Fig. 2. Continuous drain current as a function of mounting base temperature



$T_{mb} = 25°C$; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



T_j is limited to 175 °C and $T_{j(rise)}$ is limited to 30 °C

Fig. 4. Repetitive avalanche rating; avalanche current as a function of avalanche time

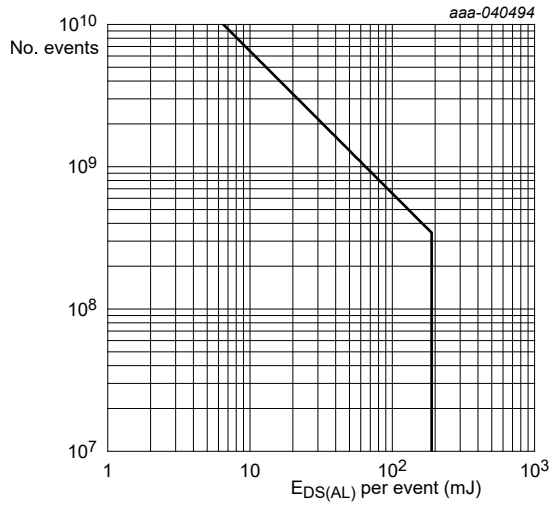


Fig. 5. Repetitive avalanche rating; maximum number of avalanche events as a function of avalanche energy

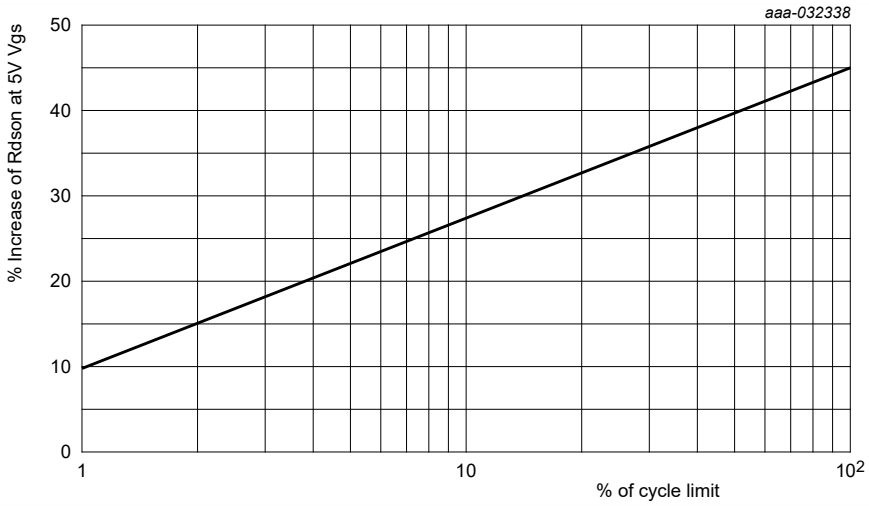
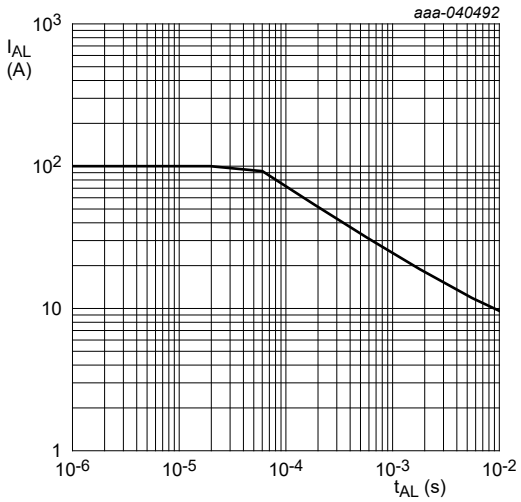


Fig. 6. Percentage Rdson at 5V increase as a function of avalanche cycles



$T_{j\ (init)}$ = 25 °C

Fig. 7. Single pulse avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	Fig. 8		-	-	0.63	K/W

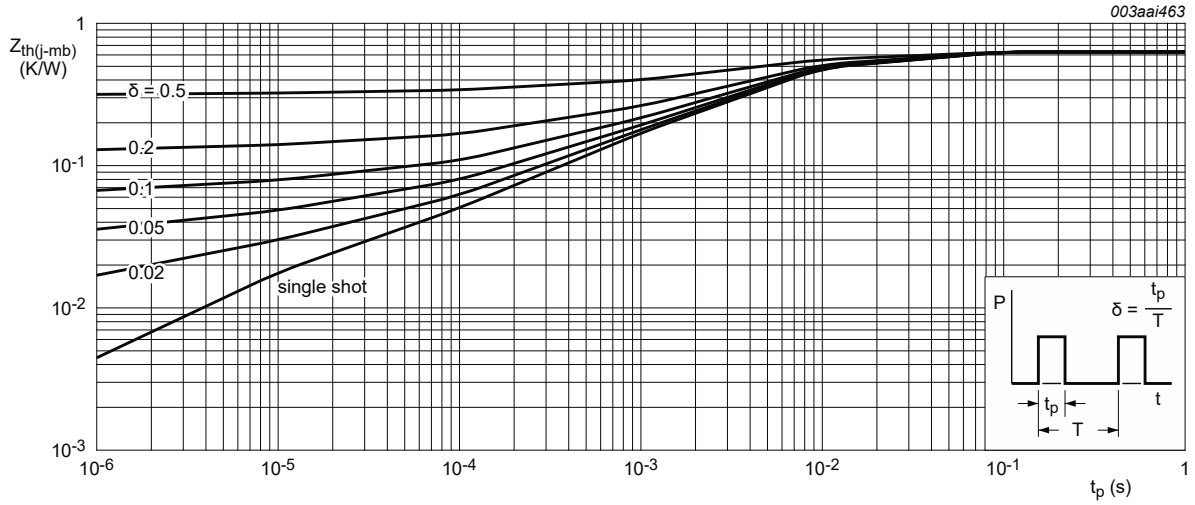


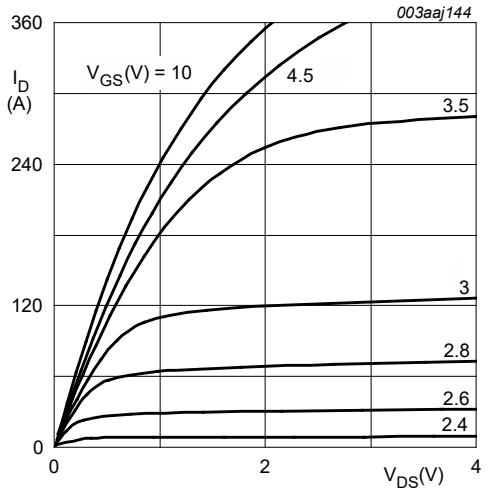
Fig. 8. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

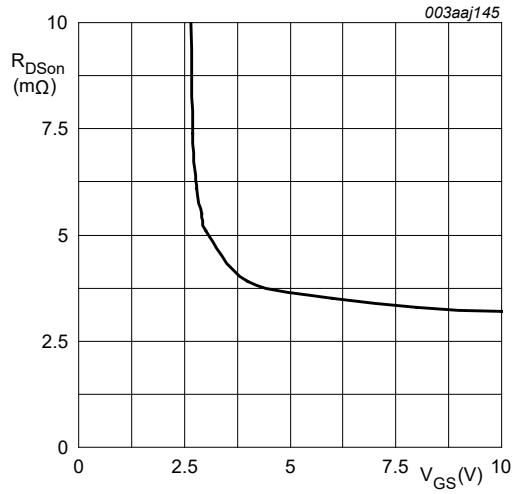
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		60	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		54	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 12; Fig. 13		1.4	1.7	2.1	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 12		-	-	2.45	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C; Fig. 12		0.5	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C		-	0.12	10	µA
		V_{DS} = 60 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A; T_j = 25 °C; Fig. 14		-	3.3	4.8	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 14		-	2.9	4.1	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 175 °C; Fig. 14; Fig. 15		-	-	10.8	mΩ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 48 V; V_{GS} = 5 V; T_j = 25 °C; Fig. 16; Fig. 17		-	54.8	-	nC
Q_{GS}	gate-source charge			-	13.6	-	nC
Q_{GD}	gate-drain charge			-	18.1	-	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 18		-	5890	7853	pF
C_{oss}	output capacitance			-	506	607	pF
C_{rss}	reverse transfer capacitance			-	276	378	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 45 V; R_L = 1.8 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	28	-	ns
t_r	rise time			-	53	-	ns
$t_{d(off)}$	turn-off delay time			-	80	-	ns
t_f	fall time			-	47	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 19		-	0.78	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V; T_j = 25 °C		-	29	-	ns
Q_r	recovered charge			-	28	-	nC



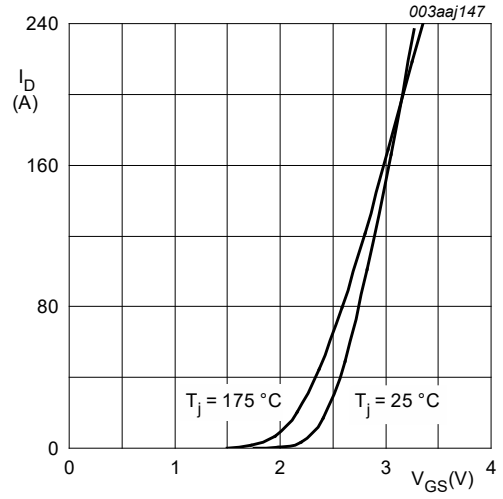
T_j = 25 °C; t_p = 300 µs

Fig. 9. Output characteristics; drain current as a function of drain-source voltage; typical values



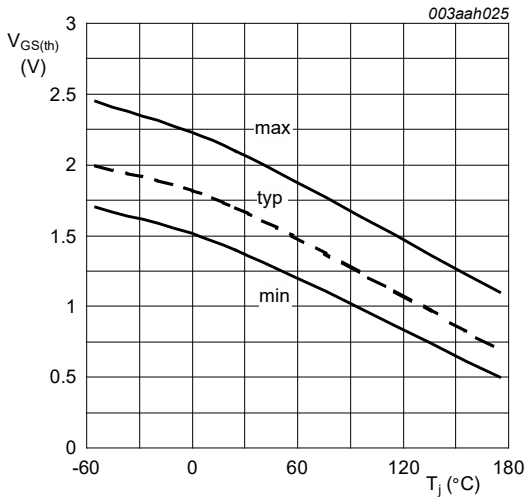
T_j = 25 °C; I_D = 25 A

Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



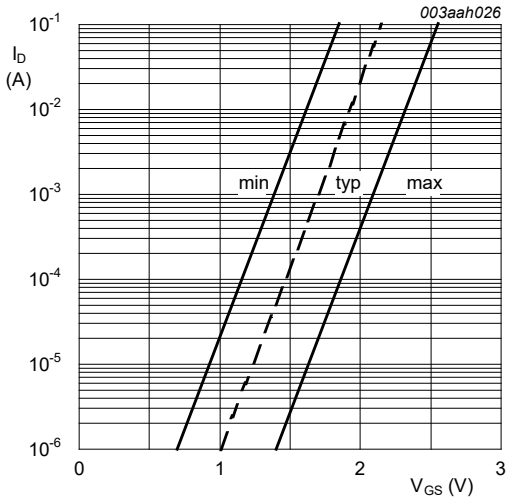
$V_{DS} = 10V$

Fig. 11. Transfer characteristics; drain current as a function of gate-source voltage; typical values



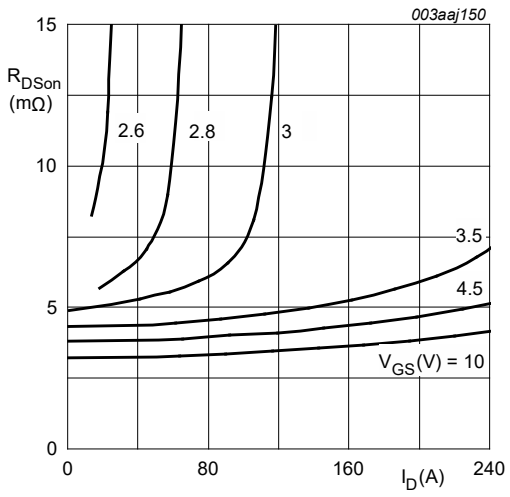
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig. 12. Gate-source threshold voltage as a function of junction temperature



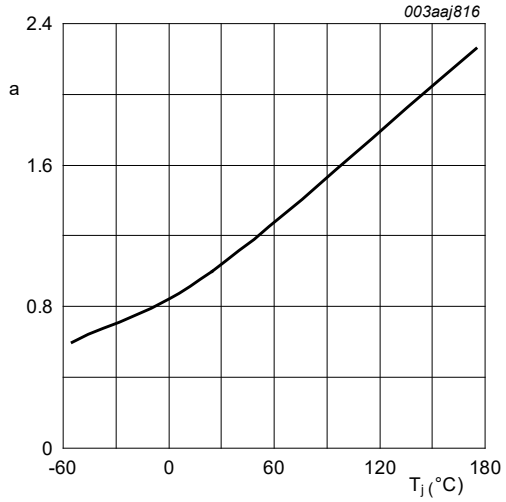
Tj = 25 °C; VDS = 5 V

Fig. 13. Sub-threshold drain current as a function of gate-source voltage



T_j = 25 °C; t_p = 300 µs

Fig. 14. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25°C)}$$

Fig. 15. Normalized drain-source on-state resistance factor as a function of junction temperature

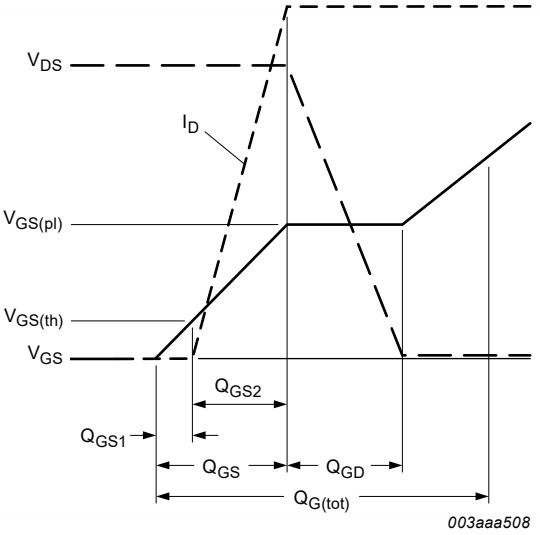
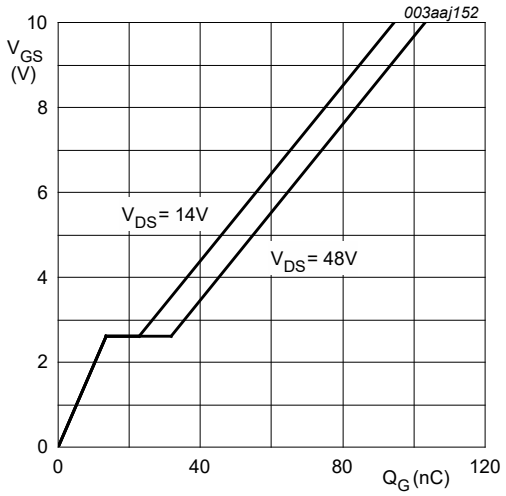
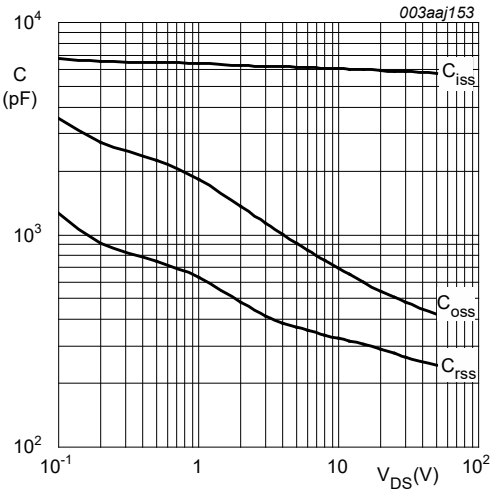


Fig. 16. Gate charge waveform definitions



$T_j = 25°C; I_D = 25A$

Fig. 17. Gate-source voltage as a function of gate charge; typical values



$T_j = 25°C; I_D = 25A$

Fig. 18. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

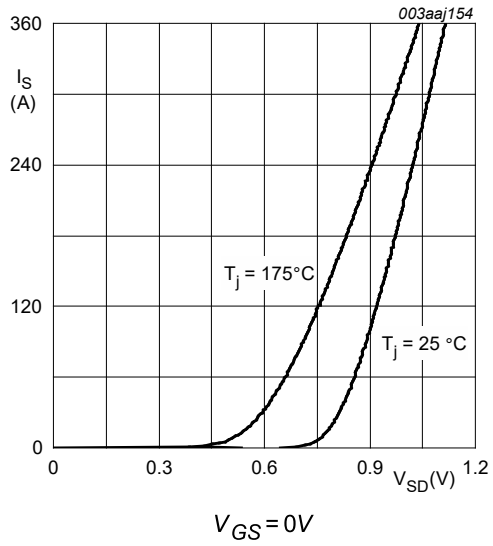
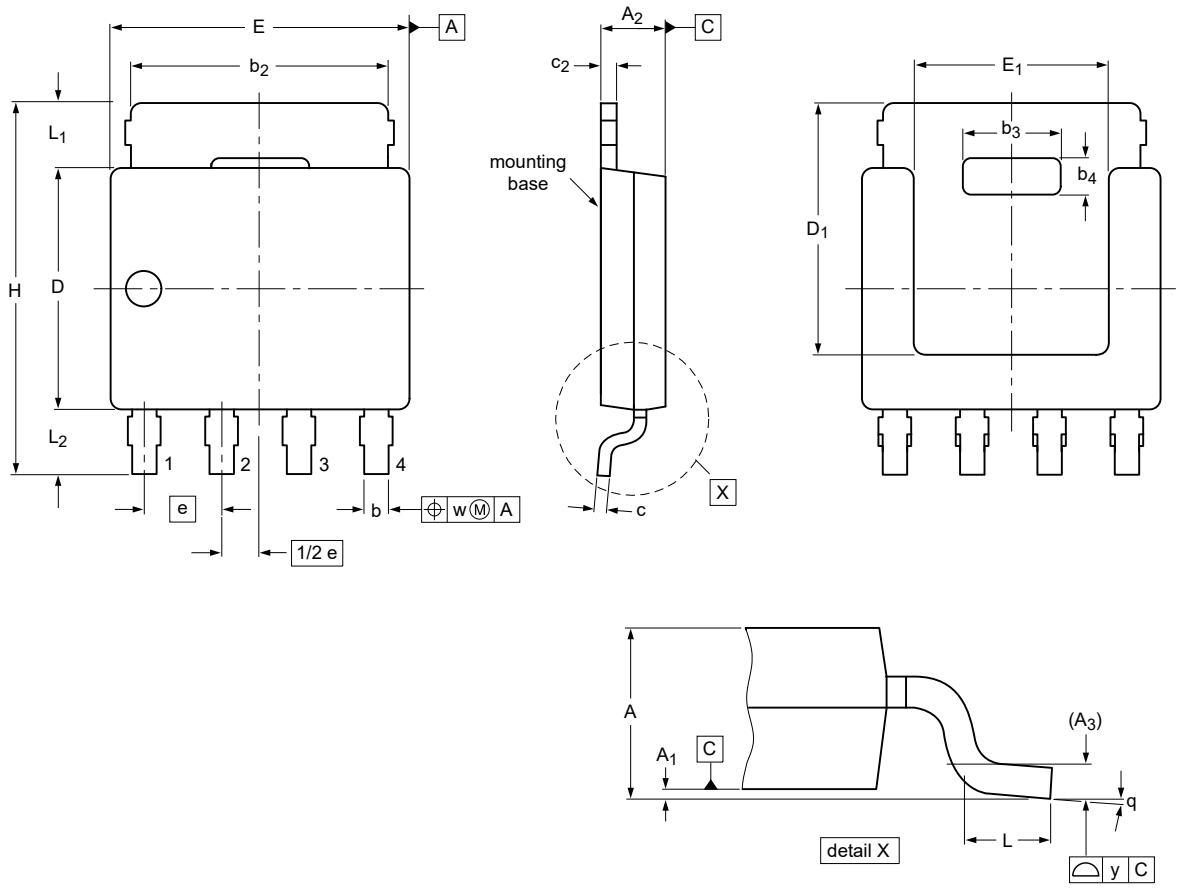


Fig. 19. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads **SOT669**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	$D^{(1)}$	$D_1{}^{(1)}$	$E^{(1)}$	$E_1{}^{(1)}$	e	H	L	L_1	L_2	w	y
mm	max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3		
	nom				0.25											1.27					0.25	0.1
	min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

θ: max 8°, nom —, min 0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~11-03-25~~ 13-02-27

Fig. 20. Package outline LFPAK56; Power-SO8 (SOT669)

12. Soldering

Footprint information for reflow soldering **SOT669**

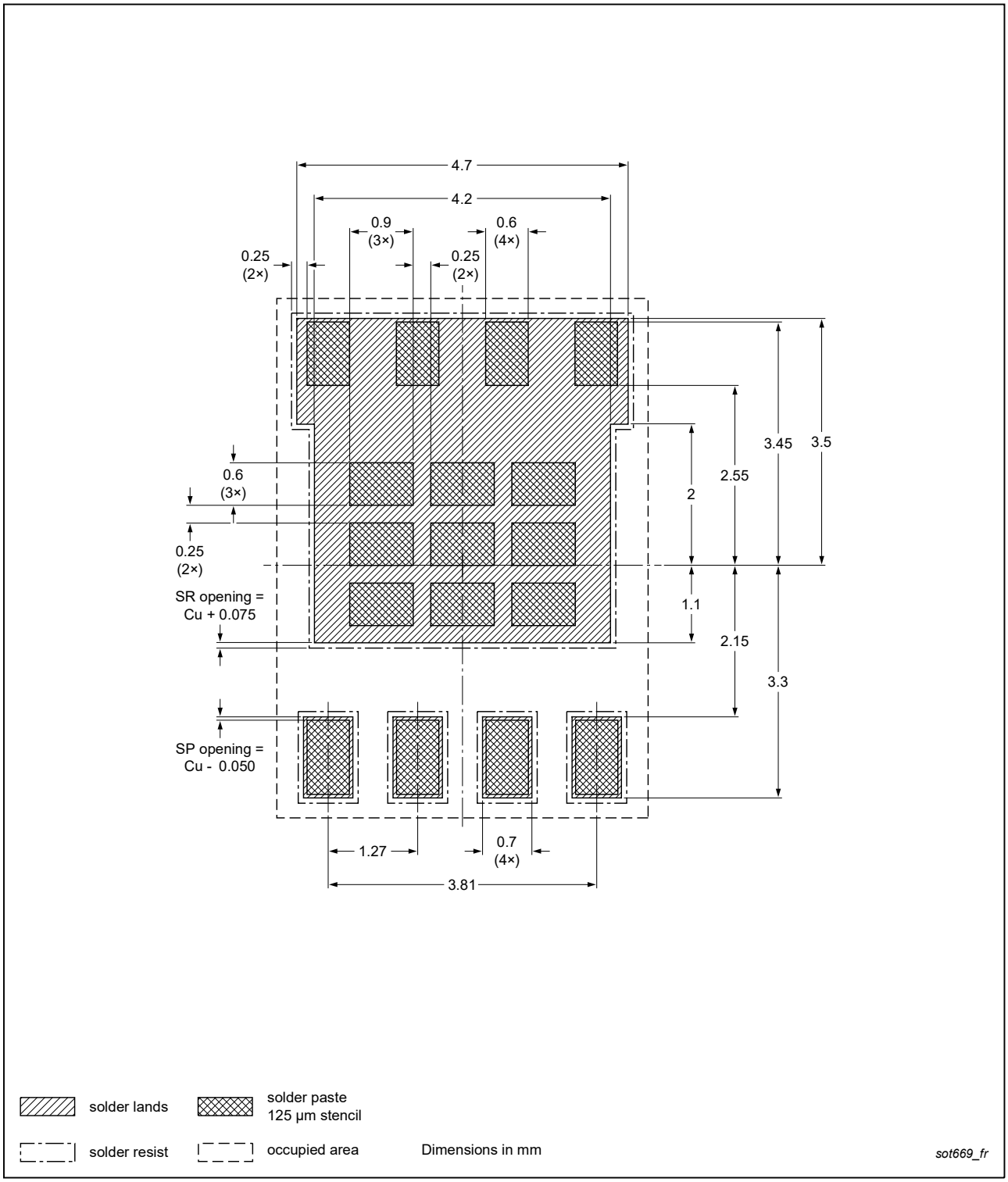


Fig. 21. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)

Wave soldering footprint information for LFPAK56 package **SOT669**

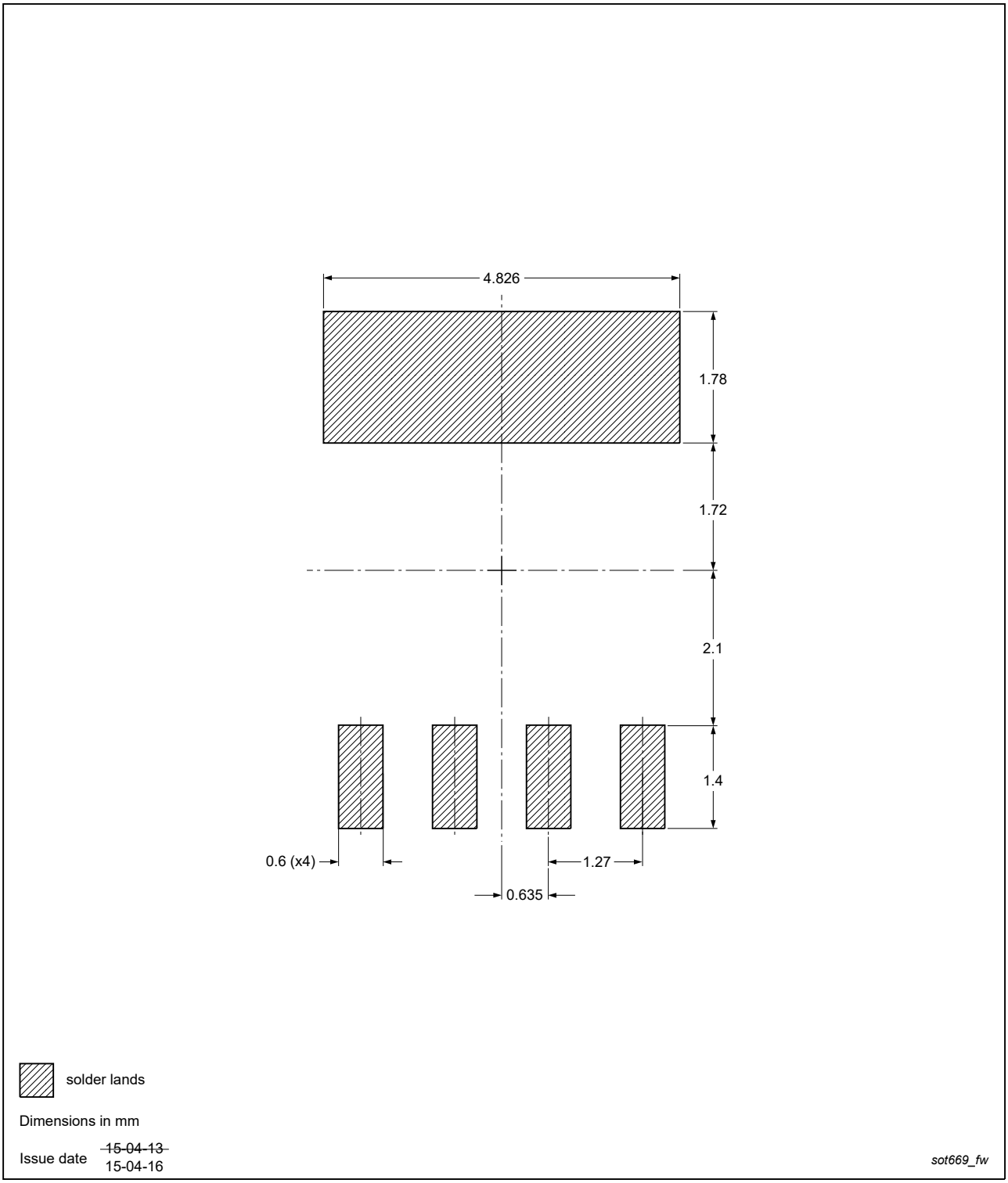


Fig. 22. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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